

PUMP ON, and SPEED LOW alarm conditions. The lower panel contains the POWER ON indicator, the MASTER/SPARE TIMING SWITCH, the MOTOR RESET pushbutton, the environmental pressure gauges and the helium bottle access door.

Drum Control Module - The drum control module controls the transfer of data between the drum and core memory. Data are written or read on the recording surface serially one bit at a time, and are transferred between the drum control module and memory in parallel, 16 bits at a time. Data transfers are in groups of four words and are conducted under program control. Transfers can be accomplished at a relatively high rate because the drum addresses memory directly without processor supervision.

Drum Control Unit Indicator Panel - The drum control unit indicator panel, located near the top front of the central processor subsystem cabinet (refer to Figure 2-7), monitors the status of the drum unit. During drum data transfers, the indicators identify track address,

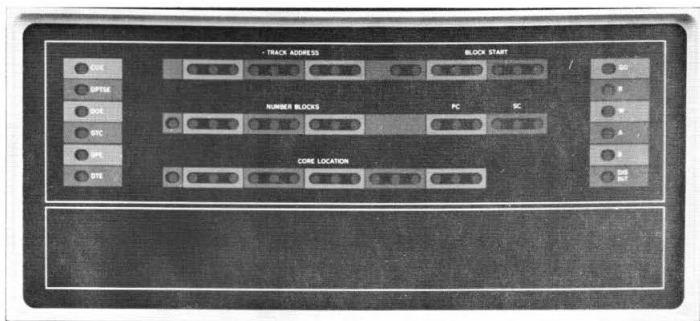


Figure 2-7. Drum Control Unit Indicator Panel

core memory location, block numbers, direction of transfer, and other pertinent data.

The indicator panel also monitors the drum operation for errors. Indicators light for core overflow, abnormal drum temperature or helium pressure, and parity and timing errors.

Data Transfer Operation - When a program requires a data transfer between the drum and memory, it enters a service routine and initializes the drum file. This initializing transmits the following information to the drum file under program control:

- a. Transfer direction - read from memory and write on disk, or read from disk and write in memory.
- b. Drum starting address - track and data block at which to start transfer.
- c. Memory starting address - core location at which to start transfer.
- d. Size of transfer - number of drum data blocks.
- e. Command to start the transfer.

When the service routine is completed, the processor continues execution of programs in the normal sequence and the drum file begins operation preliminary to executing the data transfer.

Drum Write Operation - When a data transfer is to be into the drum file, the drum control module asserts a direct memory access request (DMARQ) signal to the data bus interface module (refer to Figure 2-8). Then DBI in turn requests bus mastership for an NPR transaction, and when received, grants the DMA request to the drum control module. When the DMA request is granted, it is maintained for four memory cycles and four words read from memory are loaded into the parallel buffer registers (one word is transferred in parallel from memory to the DCM for each DMA cycle). When the DMA sequence is completed, the clock-track (block mark) data are read in search of the drum starting address.

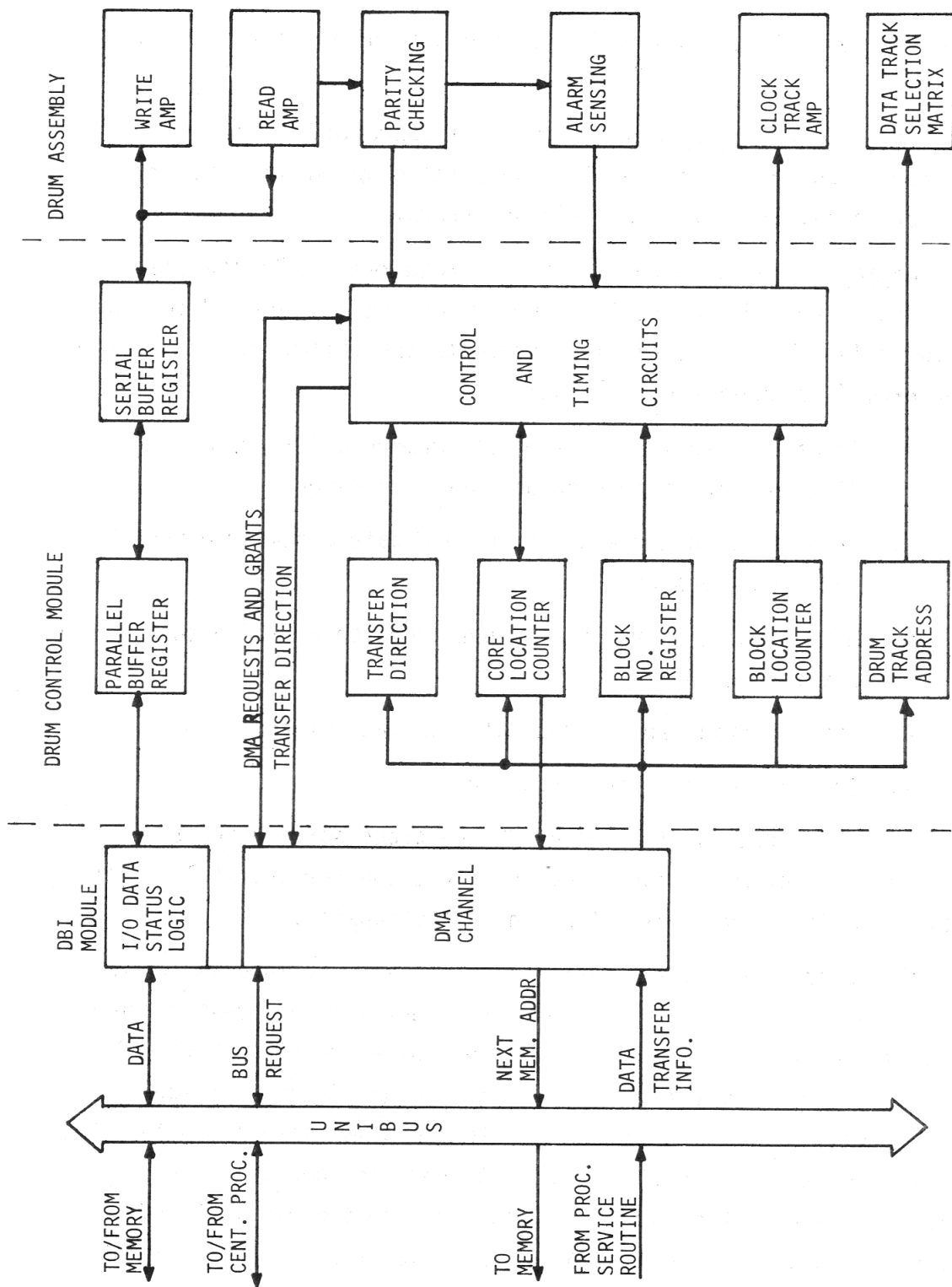


Figure 2-8. Drum File Simplified Block Diagram and Interface

When the starting data block is located, the four data words are transferred into four serial buffer registers and another DMA request is made to fetch the next four words from memory. The contents of the serial buffer registers are shifted to the write amplifier and recorded for each word. DMA requests load the parallel buffer registers while the serial buffer registers are being shifted to record. Timing of each DMA request is designed to provide the maximum time to fetch and hold data so that recording, once started, is continuous until the program-designated transfer size has been obtained. If the address of the data exceeds memory capacity, the core overflow error flag is set and the current block transfer runs to completion using the highest available memory address for each remaining DMA cycle.

Drum Read Operation - When a data transfer is to be out of the drum file, a search for the drum starting address begins as soon as operation is initiated. When the starting block is located, the first four words are read from the disk and shifted into the serial buffer register (bit-by-bit). These four 16-bit words are transferred in parallel to the parallel buffer registers and a DMA request is made. When the request is granted, it is again maintained for four memory cycles to transfer the four words to memory (one word is transferred in parallel for each memory cycle). While data are being transferred between the parallel buffer register and memory, data continue to be read serially from the disk and assembled in the serial buffer register. Parity of each word is checked in the drum assembly and the drum parity error flag is set if an odd parity is detected. Timing of each DMA request is designed to provide the maximum time to transfer data to memory so that playback, once started, is continuous until the program-designated transfer size has been obtained. The core overflow error flag is set as in a transfer into the drum file.

Standard Options - The drum file is available in either of two standard capacities as described below and may be operated on 50 Hz or 60 Hz power.

	<u>Disks</u>	<u>Surfaces</u>	<u>Heads</u>	<u>Word Capacity</u>
Option 1	1	1	64	128K
Option 2	1	2	128	256K